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(54) Receiver DC offset compensation

(57) In a receiver, e.g. for GSM, dc offset in the baseband signal output of a mixer (3) is initially estimated by closing switches (12 and 13) low pass filtering (in 14) the baseband signal to produce an estimate of the dc offset, and storing the estimate in a register (16). Switches (12 and 13) are then opened. The stored estimate is subtracted from the baseband signal in a summing amplifier (5). Residual dc offset remaining, or arising later, in the baseband signal is estimated by a residual dc offset estimator (8), and the estimate is stored in a register (9). The estimates stored in registers (9 and 16) are summed in a summer (10) prior to subtraction from the baseband signal in amplifier (5) to produce a baseband signal substantially free of dc offset enabling both the full dynamic range of A/D converter (7) to be used, and satisfactory operation of demodulator (18).

FIG. 2(A)

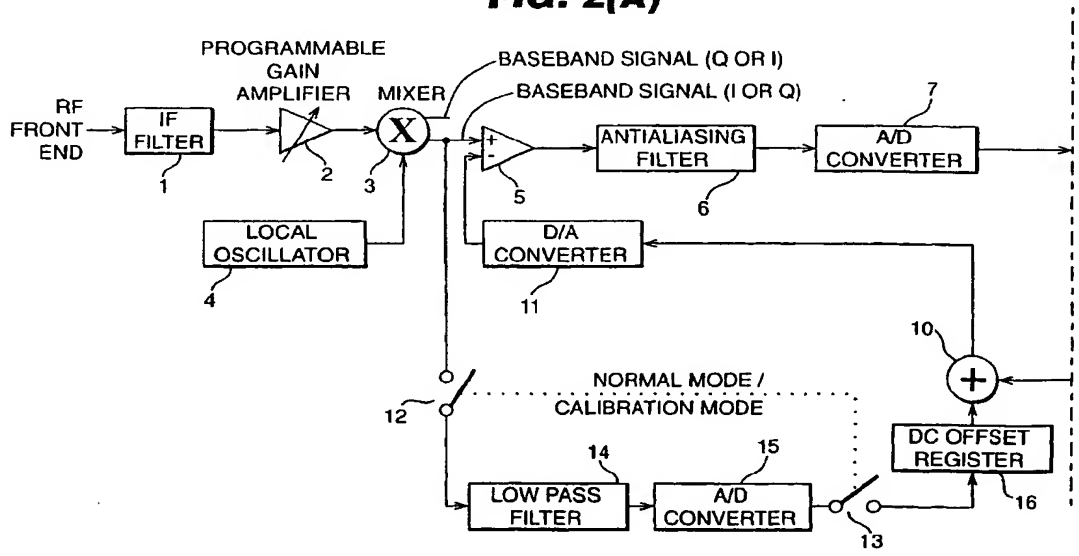

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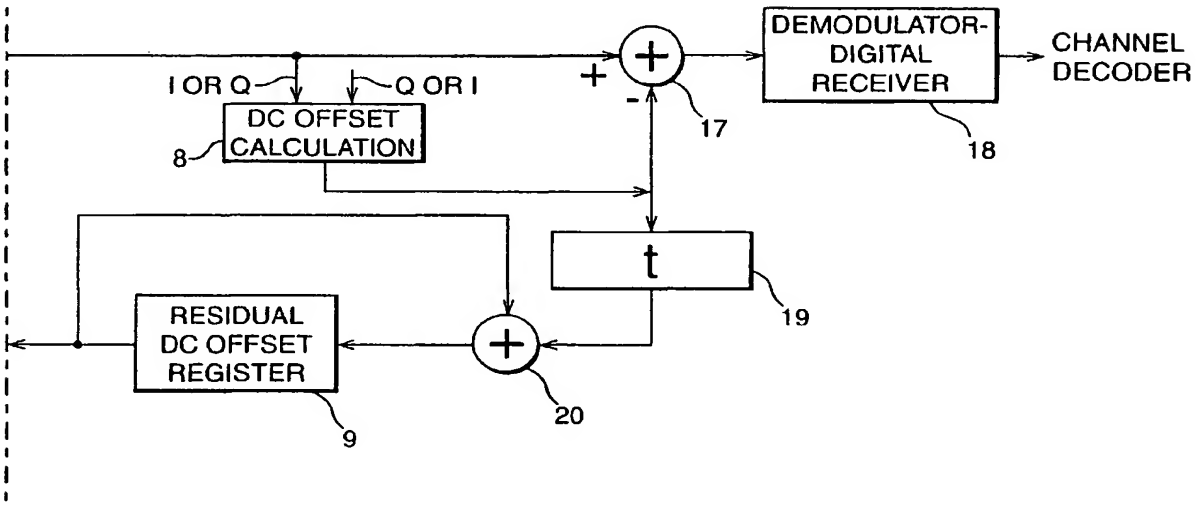
FIG.2(B)


I OR Q
Q OR I
DC OFFSET CALCULATION
8
+
-
17
DEMODULATOR-DIGITAL RECEIVER
18
CHANNEL DECODER
t
19
RESIDUAL DC OFFSET REGISTER
9
20

Description

Technical Field

[0001] This invention relates to receivers, and to methods of dc offset compensation.

Background of the Invention

[0002] In a radio receiver where an incoming signal and a local oscillator signal are mixed in a mixer to produce a baseband signal, the baseband signal will usually, and undesirably, include a dc offset component which is dependent on a number of factors such as the particular circuitry employed, temperature, and circuit gain. The dc offset arises from the local oscillator signal leaking through the mixer and mixing with itself, and from the incoming signal leaking through the mixer and mixing with itself. Dc coupled baseband amplifiers, if present, may add to the unwanted dc offset. Where the receiver includes an A/D converter fed by the baseband signal, e.g. in a Time Division Multiple Access (TDMA) receiver, the circuit gain is normally variable so as to achieve perfect excitation in the A/D converter. However, dc offset in the baseband signal reduces the useable dynamic range of the converter, and degrades the performance of a subsequent digital receiver demodulator.

[0003] In a typical TDMA receiver the dc offset is measured regularly during receive gaps, and stored as a charge on a capacitor. It is then subtracted from the baseband signal. The receiver is designed so that, although in fact the stored charge leaks away, the dc offset can be assumed constant during one timeslot. This technique will be more fully described later.

[0004] In newer TDMA systems, such as GSM, transmission and reception over multiple timeslots is possible. and it is not therefore possible to measure the dc offset regularly during receive gaps. The problem of dc offset compensation also arises in CDMA systems using baseband sampling where continuous reception over a period of time is a system requirement. In the known technique described above, the stored charge leaks away, and, because the dc offset may vary over a period of time, due for example to changes in temperature and circuit gain, the known technique is not satisfactory for application in, for example, a GSM receiver, where its use would lead to a degradation in performance.

Summary of the Invention

[0005] According to one aspect of this invention there is provided a receiver comprising a local oscillator; a mixer for mixing an incoming signal and output from the local oscillator to produce a baseband signal; a dc offset estimator for providing an estimate of the dc offset in the baseband signal in the absence of the incoming signal to the mixer; a first register for storing the estimated dc offset; a subtraction circuit for subtracting the stored estimate from the baseband signal; and a residual dc offset estimator for estimating residual dc offset in the baseband signal, for subtraction from the baseband signal by the subtraction circuit.

[0006] In one embodiment the first register is a digital register; and the dc offset estimator comprises a low pass filter for filtering the baseband signal to produce an estimate of the dc offset, and an A/D converter for converting the estimate to digital form for storage in the first register.

[0007] In another embodiment the first register is a digital register; and the dc offset estimator comprises means for producing in digital form a series of successive approximations of the dc offset until the dc offset is substantially estimated, and for storing the dc offset in the first register.

[0008] There may be provided a second register for storing the estimated residual dc offset. There may be provided a summer for summing the stored dc offset estimate and the stored residual dc offset estimate; wherein the subtraction circuit comprises a subtractor for subtracting the summed estimates from the baseband signal. The subtractor may be a baseband amplifier. The second register may be a digital register, and there may be provided a D/A converter for converting the summed estimates to analog form before application to the subtractor.

[0009] There may be provided a summer having an output which feeds the input of the second register, and inputs which are fed. respectively. by output of the second register and the residual dc offset estimate from the residual dc offset estimator. thereby to update the estimate stored in the second register.

[0010] Output from the residual dc offset estimator may be fed to the second register via a delay element, and directly to one input of a subtractor having another input fed by output from the subtraction circuit.

[0011] The said one embodiment of the receiver may comprise an A/D converter for receiving output from the subtraction circuit; wherein the residual dc offset estimator is fed by output from the A/D converter.

[0012] The said other embodiment of the receiver may comprise an A/D converter for receiving output from the subtraction circuit; wherein the dc offset estimator and the residual dc offset estimator are fed by output from the A/D converter.

[0013] There may be provided a switch for isolating the input and the output of the dc offset estimator after estimation

of the dc offset.

[0014] According to another aspect of this invention there is provided a method of compensating for dc offset in the baseband signal output of a mixer fed by an incoming signal and a local oscillator signal, comprising: estimating the dc in the baseband signal in the absence of the incoming signal to the mixer; storing the estimated dc offset in a register; estimating residual dc offset in the baseband signal; and subtracting the stored estimate and the residual dc offset from the baseband signal.

Brief Description of the Drawings

[0015] The invention will now be described by way of example with reference to the accompanying drawings, in which:

FIG. 1 is a schematic diagram of part of a TDMA receiver employing a known dc offset compensation technique: FIG.2 shows the relationship between FIGS.2A and 2B which are a schematic diagram of part of a receiver embodying the invention, and the relationship between FIGS. 2C and 2D which are a schematic diagram of part of another receiver embodying the invention; and

FIGS. 3 to 9 are various flow and other diagrams referred to in an Appendix hereto describing three ways of estimating dc offset, FIG.4 showing the relationship between FIGS. 4A and 4B.

Detailed Description

[0016] Referring now to Fig. 1, a signal from the receiver front end (not shown) is filtered in an IF filter 1, amplified in a programmable gain amplifier 2, and applied as one input to a mixer 3 whose other input, supplied by a local oscillator 4, is at a frequency whereby the mixer output is at baseband. Normally, the mixer output comprises both I and Q components, but for the sake of clarity only one component, and the associated circuitry, will be considered.

[0017] Due to the action of the mixer, the baseband output may contain a dc offset, the magnitude of which may be dependent on factors such as temperature, and the gain of amplifier 2. The baseband output is applied to the positive input of a summing amplifier 5 whose output is fed to an antialiasing filter 6 which in turn feeds an A/D converter 7. The output of A/D converter 7 is fed to a demodulator or digital receiver 18. Any dc offset in the baseband signal reduces the useable dynamic range of the A/D converter 7, and degrades the performance of the demodulator 18 and any subsequent channel decoder (not shown). Summing amplifier 5 itself may introduce an additional dc offset to the baseband signal.

[0018] In order to compensate for the dc offset, the dc offset is estimated regularly, and a signal representative of it is applied to the negative input of summing amplifier 5 so as to compensate for the dc offset prior to the A/D converter 7.

[0019] Estimation of the d.c. offset is usually done during receive gaps as follows. The input to the amplifier 2 is grounded so as to shunt any signal from the RF front end to ground. A normally open switch 12 is closed, i.e. it is switched to the calibration mode, and a low pass filter 14 filters out the dc offset in the baseband signal. The charge acquired on a capacitor in filter 14 is an estimate of the dc offset and is applied to the negative input of amplifier 5 which subtracts the estimate from the baseband signal. After each estimation of the dc offset, the input to amplifier 2 is ungrounded, switch 12 is opened, and normal reception is resumed.

[0020] As noted earlier, where mixer 3 provides both I and Q output components, a further summing amplifier 5, filter 6, A/D converter 7, switch 12 and low pass filter 14, none of which is shown, are required to process the other component.

[0021] This solution suffers from the defect that the charge on the capacitor leaks away, and thus the dc offset estimate applied to amplifier 5 varies over time. Furthermore, any dc offset due to mixing of the IF signal with itself in mixer 3 will not be accounted for because the input to amplifier 2 is grounded during dc offset estimation.

[0022] In newer TDMA systems, such as GSM, where reception and transmission over multiple timeslots is possible, regular estimation of the dc offset during receive gaps is not possible, and because of this and because the stored charge leaks away, and because the dc offset is gain and temperature dependent, and thus may vary over time, dc offset compensation as described above is unsatisfactory. It is also not suitable in CDMA systems using baseband sampling where continuous reception over a period of time is a system requirement.

[0023] Referring now to Figs. 2A and 2B, the operation of filter 1, amplifier 2, mixer 3 and local oscillator 4 are as previously described with reference to Fig. 1. In Figs. 2A and 2B, however, dc offset compensation is effected as follows.

[0024] An initial dc offset estimate is required because the dc offset in the baseband signal output of mixer 3 may be a significant, or even the major, component of the baseband signal. A dc offset of significant magnitude may swamp the A/D converter 7 and cause it to give an erroneous output, with a consequent deleterious effect on subsequent circuit elements.

[0025] Initial dc offset estimation is effected by grounding the input to amplifier 2. Switches 12 and 13 are closed, i. e. switched to the calibration mode, and a low pass filter 14 filters out the dc offset in the baseband signal. The charge

acquired on a capacitor in filter 14 is an estimate of the dc offset and is converted to digital form by an A/D converter 15 and stored in a dc offset register 16. The input to amplifier 2 is then ungrounded and switches 12 and 13 are opened, i.e. switched to the normal mode. The estimate stored in register 16 is applied via summer 10, of which more later, to a D/A converter 11 which provides an analog version of the stored dc offset estimate to the negative input of summing amplifier 5, which in turn subtracts the dc offset estimate from the baseband signal. The output of amplifier 5 is provided, via an antialising filter 6, to an A/D converter 7 whose output feeds a demodulator or digital receiver 18 and channel decoder (not shown). Removal of the dc offset from the baseband signal enables the full dynamic range of the A/D converter 7 to be used, and avoids degrading the performance of the demodulator 18. Because the dc offset estimate is stored in register 16, subsequent charge leakage in the capacitor in filter 14 is of no effect.

[0026] As noted earlier however, it is not feasible to estimate the dc offset regularly in receive gaps in newer TDMA systems, such as GSM, where multiple timeslot operation is contemplated, and thus any residual dc offset arising, or remaining, after the initial estimation will affect the performance of A/D converter 7 and demodulator 18. Residual dc offset in the baseband signal, e.g. due to changes in gain or temperature, is estimated by a residual dc offset estimator 8, and the estimate is stored, after a time delay in delay 19, in a residual dc offset register 9. Estimator 8 may be a processor adapted to operate under the control of a suitable algorithm to produce an estimate of the residual dc offset. Three ways of estimating the residual dc offset are given by way of example in the Appendix hereto. It will be noted that estimator 8 requires both I and Q inputs to perform the exemplary algorithms.

[0027] The estimate stored in register 9 is summed in summer 10 with the estimate stored in register 16, and the sum is converted to analog form in D/A converter 11 whose output is subtracted from the baseband signal in amplifier 5 to provide an output which is substantially free of dc offset. A summer 20 is fed with output from register 9 and output from time delay 19 so as to update register 9 as changes in the residual dc offset occur. The output of estimator 8 also feeds a subtractor 17 so that changes in the residual dc offset can be subtracted instantaneously from the signal fed to the demodulator 18. The delay provided by time delay 19 is chosen so as to prevent the residual dc offset estimate produced by estimator 8 from being subtracted twice over, once in amplifier 5, and again at the output of A/D converter 7.

[0028] As noted earlier, estimator 8 is fed with both I and Q input components. For the sake of clarity Figs. 2A and 2B show only the circuit elements for processing one of these components; for processing the other component a further set of components 5 to 7, 9 to 17 and 19 is required.

[0029] It will thus be understood that the demodulator 18 will always receive a signal substantially free of dc offset, and the useable dynamic range of A/D converter 7 will be maximised.

[0030] When switches 12 and 13 are open. i.e. in the normal mode, power saving may be achieved by de-energising filter 14 and A/D converter 15. Further power savings may be made if there is no change in the residual dc offset, or if any changes are slow and small, by estimating the residual dc offset less frequently.

[0031] Variations will, of course, occur to those skilled in the art. For example, switch 12, shown connected to the output of mixer 3, could instead be connected to the output of summing amplifier 5. The initial dc offset estimation would then take into account any dc offset introduced by amplifier 5 itself. Furthermore, instead of summing the outputs of registers 9 and 16. the contents of these registers could be individually subtracted from the baseband signal, e.g. by summing amplifier 5 subtracting only the dc offset estimate, and another subtractor fed with output from amplifier 5 for subtracting the residual dc offset estimate after any necessary D/A conversion.

[0032] Another receiver embodying the invention will now be desribed with reference to FIGS. 2C and 2D in which components bearing the same reference signs as those in FIGS. 2A and 2B perform corresponding functions as already described. The main difference between the receiver of FIGS. 2A and 2B and the receiver of FIGS. 2C and 2D lies in the manner in which the initial DC offset is estimated.

[0033] To estimate the initial DC offset, switches 12 and 13 are closed and switch 21 is opened, the input to amplifier 2 being grounded as before. Offset calculation logic 22 includes a comparator (not shown) which is fed with output from the A/D converter 7 and which provides a signal representative of whether the DC offset in the A/D converter's output is positive. negative, or zero. Offset calculation logic 22 also includes logic circuitry (not shown) which provides to D/A converter 11 an offset compensation signal dependent upon whether the comparator output represents a positive or negative DC offset. The output of D/A converter 11 is subtracted in amplifier 5 from the baseband signal, and the output of A/D converter 7 is again examined by the comparator in offset calculation logic 22 to repeat the process just described. The process is repeated until, by a series of successive approximations, the compensation signal provided to the D/A converter 11 is such as to substantially cancel the DC offset in the baseband signal. At this point, the comparator in offset calculation logic 22 provides a signal representative of zero DC offset and the process of successive approximations is stopped. Switches 12 and 13 are opened and a digital representation of the DC offset at the output of offset calculation logic 22 is low-pass filtered in a noise filter 14' and stored in DC offset registers 16' in response to a latch signal on lead 23 from offset calculation logic 22. Logic circuitry suitable for performing the functions of offset calculation logic 22 will be well-known to those skilled in the art, and will not be described further.

[0034] After the initial DC offset estimation is complete, switch 21 is closed, and subsequent operation is as already described with reference to FIGS. 2A and 2B. Thus, any residual DC offset arising. or remaining, after the initial esti-

mation is estimated by residual DC offset estimator 8, and the estimate is stored, after a time delay in delay 19, in residual DC offset register 9. The estimate stored in register 9 is summed in summer 10 with the estimate stored in registers 16', and the sum is converted to analog form in D/A converter 11 prior to subtraction from the baseband signal in amplifier 5 to provide an output which is substantially free of DC offset.

[0035] As noted earlier, the DC offset is dependent upon the gain of programmable gain amplifier 2, and thus may vary for different gain settings. By performing for each of the gain settings of amplifier 2 an initial DC offset estimation in the manner described. it is possible to store a corresponding DC offset estimate in DC offset registers 16'. Thus, DC offset registers 16' effectively constitute a form of look-up table which provides to summer 10 the DC offset estimate appropriate to the gain setting of amplifier 2 in accordance with a "gain select" signal on lead 24. Storing a plurality of DC offset estimates avoids the need to perform an initial DC offset estimation process each time the gain of amplifier 2 is changed.

Appendix: DC offset compensation

The basic technique of DC offset compensation is to subtract a calculated DC offset (output of block 8 in Figure 2A) from the incoming signal .

Certain uncommon expressions (derotating, midamble, burst, channel impulse response, quadrant) are necessary for explaining this technique in detail.

Usually, the receiver "**derotates**" the incoming signal before the process of recovering the user bits is commenced. Derotating is multiplying the I/Q symbols of the incoming signal with a certain factor. This factor is complex and depends on the time or the index of the symbol, respectively (Equation 1). Equation 1 can be written as Equation 2. Derotating in Equation 7 takes also the phase error into consideration.

$$I_{derot,k} + j \cdot Q_{derot,k} = (I_k + j \cdot Q_k) \cdot \exp(j \cdot \frac{\pi}{2} \cdot k)$$

Equation 1

$$I_{derot,k} = \cos(j \cdot \frac{\pi}{2} \cdot k) \cdot I_k - \sin(j \cdot \frac{\pi}{2} \cdot k) \cdot Q_k$$

$$Q_{derot,k} = \sin(j \cdot \frac{\pi}{2} \cdot k) \cdot I_k + \cos(j \cdot \frac{\pi}{2} \cdot k) \cdot Q_k$$

Equation 2

Equation 1 is explained in more detail since it will be helpful to understand the "-1/1 version of the midamble" described later. Equation 1 gives more graphical impression which effect is taken by the complex exponential factor on the phase of the I/Q symbols. In the ideal case of GSM the difference of the phase of two consecutive incoming symbols is either $+\pi/2$ or $-\pi/2$. After derotating, the difference of the phase is either π or 0. Figure 3 shows the effect of derotating for example symbols in the complex Gaussian plane. Here, $I_k+j \cdot Q_k$ may lie in any of the four **quadrants** of the Gaussian plane - after derotation, only two quadrants may be occupied.

The transmission of signals is never ideal. Unwanted effects impair the signal during trans/from the sender to the receiver. The "**midamble**" makes it possible to estimate and reduce those unwanted effects in the receiver. For that, a couple of bits are grouped. A sequence of bits which are known to the sender and the receiver are inserted in the middle of this group. The sequence of known bits is called midamble. The whole group of bits after inserting is called "**burst**".

Derotating results in two possible states for the symbols (Figure 3). To adapt the midamble to those two states, it is transformed into a "**-1/1 midamble**" by assigning the values –1 and 1 to the bit states zero and one.

During transmission from the sender to the receiver the known midamble bits are modified in the same way as the unknown bits. Since the receiver knows what the midamble should be, it is able to estimate in which way the signal has been modified. This estimation results in a "**channel impulse response**".

With the help of the expressions explained above, three ways for estimating the DC offset will now be explained.

First way of DC offset estimation

A very simple way of estimating the DC offset is based on the average value of the received I- and Q-signals (Equation 3). Note that the DC offset of Equation 3 is not only caused by the mixers but also by the unequal distribution of bit states.

$$\text{DC offset} = \frac{1}{2 \cdot 148}\left(\sum_{k=1}^{148} I_{rec,k} + \sum_{k=1}^{148} Q_{rec,k}\right)$$

Equation 3

Second way of DC offset estimation

The second way of DC offset estimation is more precise in comparison to the first way – only the DC offset caused by the mixers is estimated. But it needs more calculation power in comparison to the first way.
The incoming signal consists of not derotated received bursts. DC offset calculation (block 8 in Figure 2B) adds a DC offset to a not-derotated received burst (block 24 in Fig.4A), derotate it (25) and compare its midamble (calculated derotated midamble) with the received derotated midamble (28). This procedure is repeated with different DC values until a certain criterion, based on the difference between the calculated and the received midamble, is minimal (34). The DC offset found in this way is the result of block 8 in Figure 2B. A detailed description follows.

Set of DC offsets (22), (33)

The initial set of DC offsets is based on the average value of the I and Q signals of a received burst (Equation 4, see item 22 in Figure 4A).

$$\text{initial set of DC offsets} = \frac{1}{2 \cdot 148}\left(\sum_{k=1}^{148} I_{rec,k} + \sum_{k=1}^{148} Q_{rec,k}\right) + \{-8.8\ -4.4\ -2.2\ -1.1\ -0.11\ 0.1\ 1\ 2\ 4\ 8\}$$

Equation 4

After each iteration the set of DC offsets is modified and defined as a distribution around the best DC offset of the previous iteration (33). The width of the distribution depends on the criterion of the previous iteration (Equation 5).

$$\text{set of DC offsets} = (\text{best DC offset of previous iteration}) + |\text{criterion value}| \cdot \{-2.2\ -1.1\ -0.11\ -0.011\ 0.01\ 0.1\ 1\ 2\}$$

Equation 5

Add received burst and DC offset (24)

Equation 6 describes the adding operation (block 24 in Figure 4A).

$$I_{add,k} + j \cdot Q_{add,k} = I_{rec,k} + j \cdot Q_{rec,k} + \text{DC offset} \cdot (1 + j)$$

Equation 6

Derotating (25) / detection of the correct quadrant (21)

Derotating is a continuing process. If the current phase offset is not known/memorised, it has to be determined. Here, the correct quadrant is sufficient. For that, the received burst is derotated with four different additional constants k_{offs}=0,1,2,3, one for each quadrant (Equation 7). The k_{offs} with the minimum difference between the just calculated $I_{derot,k,koffs}+j \cdot Q_{derot,k,koffs}$ and the earlier calculated $I_{derot,k}+j \cdot Q_{derot,k}$ is chosen. The difference for each k_{offs} is described in Equation 8.

$$I_{derot,k,koffs} = \cos\left((\frac{\pi}{2} + \frac{\text{phase error}}{\text{symbol}}) \cdot (k + k_{offs})\right) \cdot I_{add,k} - \sin\left((\frac{\pi}{2} + \frac{\text{phase error}}{\text{symbol}}) \cdot (k + k_{offs})\right) \cdot Q_{add,k}$$

$$Q_{derot,k,koffs} = \sin\left((\frac{\pi}{2} + \frac{\text{phase error}}{\text{symbol}}) \cdot (k + k_{offs})\right) \cdot I_{add,k} + \cos\left((\frac{\pi}{2} + \frac{\text{phase error}}{\text{symbol}}) \cdot (k + k_{offs})\right) \cdot Q_{add,k}$$

Equation 7

$$\text{difference}(k_{offs}) = \sum_{k=1}^{148} \left| I_{derot,k,koffs} - I_{derot,k} + j \cdot (Q_{derot,k,koffs} - Q_{derot,k}) \right|$$

Equation 8

Calculate channel impulse response (26)

For calculating the channel impulse response (Figure 5) the -1/1 midamble is required. The exchange of the zero bits of the reference midamble with minus ones yields the -1/1 midamble. The convolution of the mirrored midamble of the received derotated burst with the middle part of the -1/1 midamble yields cross correlation values. The six consecutive cross correlation values with the highest energy are the channel impulse response.

Since the channel impulse response (and so the calculated derotated midamble) depends on the received derotated burst (and especially on the added DC offset), the DC offset is calculated iteratively, here.

Since the channel impulse response is estimated, the resulting DC offset is estimated, too.

Calculated midamble (27)

The convolution of the channel impulse response (26) with the -1/1 midamble yields to the calculated derotated midamble (Figure 6).

Calculate criterion value (28)

Calculating the criterion value requires a scaling (Figure7)of the calculated derotated midamble (Figure 6) with the help of the received derotated midamble (Figure 5).

The scaling performed in calc_scale_factor() of the AT&T GSM Digital Receiver is sufficient for the features available. For calculating a DC offset and the SNR, scaling has to be more adequate (Equation 9, Figure 7).

$$MI_{scal} + j \cdot MQ_{scal} := (MI_{cal} + j \cdot MQ_{cal}) \cdot \text{fact}$$

with

$$\text{fact} = \frac{\sum_{k=midfrom}^{midupto} \left| MI_{rec,k} + j \cdot MQ_{rec,k} \right|}{\sum_{k=midfrom}^{midupto} \left| MI_{cal,k} + j \cdot MQ_{cal,k} \right|}$$

$MI_{scal} + j \cdot MQ_{scal}$: scaled calculated derotated midamble

$MI_{cal} + j \cdot MQ_{cal}$: calculated derotated midamble

$MI_{rec} + j \cdot MQ_{rec}$: received derotated midamble

Equation 9

The DC offset criterion *dcc* is defined as the average of the absolute difference between the scaled calculated and the received derotated midamble (Equation 10).

$$dcc = \frac{1}{\sqrt{2}} \sum_{k=midfrom}^{midupto} \left| MI_{scal} - MI_{rec} + j \cdot (MQ_{scal} - MQ_{rec}) \right|$$

Equation 10

Statistics for break condition (32),(34)

After a criterion value has been calculated for every element of the set of DC offsets, the DC offset with the best criterion value is chosen and memorised (30),(31). The average of the last three criterion values is stored in "crit_mean".

The iteration is continued as long as

- "crit_mean" is less than or equal to "crit_mean" of the previous iteration, and
- the absolute difference of the last two criterion values is greater than 1e-3

Choice of DC offset (35)

After the last iteration or when the break condition is fulfilled (34), the DC offset with the best of all stored criterion values is chosen.

Compensate DC offset

The chosen DC offset (35) is subtracted from the received burst (Equation 6) and then derotated (Equation 7). If the phase for derotation is not memorised, the phase is used as determined in Equation 7, item 21.

Third way of DC offset estimation

The third way of DC offset estimation is more precise in comparison to the first way – only the DC offset caused by the mixers is estimated. It is about as precise as the second way. It needs only slightly more calculation power in comparison to the first way and much less in comparison to the second way.

In the ideal case, the symbols of the received (not derotated) burst are situated in the locations 1, j, -1 and –j within the complex Gaussian plane. Altering by a frequency shift / causes the locations to be situated on a circle. Additionally, White Gaussian Noise, fading etc. yields to locations which are distributed in an area around the circle (Figure 8). An additional DC offset shifts only the circle without changing the relative locations of the symbols to the circle.

The third way of DC offset estimation determines the centre of the circle assuming that the deviation of the locations relative to the circle is distributed normally. A detailed algorithm, which has been applied successfully, follows.

At first, the mean value of all symbols of a burst is chosen as an initial point within the circle (Equation 11).

$$\text{initial centre} = \frac{1}{148}\left(\sum_{k=1}^{148} I_{rec.k} + j \cdot Q_{rec.k}\right)$$

Equation 11

Figure 9 shows the search for a centre. After calculating the provisional centres (37) the corresponding criterion values have to be found (38). For that, the absolute distances from a centre to the locations of the symbols are calculated (Equation 12).

$$|r_k| = |I_{rec,k} + j \cdot Q_{rec,k} - \text{provisional centre}|$$

Equation 12

The criterion value for one provisional centre is the standard deviation of the absolute distances |rk| (item 38 in Figure 9). Equation 12 and the standard deviation has to be calculated four times in each iteration. The iteration is continued until the result of Equation 13 is true (item 41 in Figure 9).

$$\frac{|\text{difference of criterion values of current and previous iteration}|}{\text{criterion value of current iteration}} > 0.00018$$

&

criterion value of current iteration < criterion values of previous iteration

Equation 13

If a real DC offset has to be estimated the DC offet is the mean value of real(centre)+imag(centre).

Claims

1. A receiver comprising:

   a local oscillator;
   a mixer for mixing an incoming signal and output from the local oscillator to produce a baseband signal;
   a dc offset estimator for providing an estimate of the dc offset in the baseband signal in the absence of the incoming signal to the mixer;
   a first register for storing the estimated dc offset;
   a subtraction circuit for subtracting the stored estimate from the baseband signal; and
   a residual dc offset estimator for estimating residual dc offset in the baseband signal. for subtraction from the baseband signal by the subtraction circuit.

2. A receiver as claimed in claim 1 wherein:

   the first register is a digital register; and
   the dc offset estimator comprises a low pass filter for filtering the baseband signal to produce an estimate of the dc offset, and an A/D converter for converting the estimate to digital form for storage in the first register.

3. A receiver as claimed in claim 1 wherein:

   the first register is a digital register; and
   the dc offset estimator comprises means for producing in digital form a series of successive approximations of the dc offset until the dc offset is substantially estimated. and for storing the estimated dc offset in the first register.

4. A receiver as claimed in claim 1,2 or 3 comprising a second register for storing the estimated residual dc offset.

5. A receiver as claimed in claim 4 comprising a summer for summing the stored dc offset estimate and the stored residual dc offset estimate;

wherein the subtraction circuit comprises a subtractor for subtracting the summed estimates from the baseband signal.

6. A receiver as claimed in claim 5 wherein the subtractor is a baseband amplifier.

7. A receiver as claimed in claim 5 or 6 wherein:

the second register is a digital register;
and there is provided a D/A converter for converting the summed estimates to analog form before application to the subtractor.

8. A receiver as claimed in claim 4,5,6 or 7 comprising a summer having an output which feeds the input of the second register, and inputs which are fed, respectively, by output of the second register and the residual dc offset estimate from the residual dc offset estimator, thereby to update the estimate stored in the second register.

9. A receiver as claimed in any one of claims 4 to 8 wherein output from the residual dc offset estimator is fed to the second register via a delay element, and directly to one input of a subtractor having another input fed by output from the subtraction circuit.

10. A receiver as claimed in any one of claims 1 to 9 comprising an A/D converter for receiving output from the subtraction circuit:

wherein the residual dc offset estimator is fed by output from the A/D converter.

11. A receiver as claimed in any one of claims 1 and 3 to 9, comprising an A/D converter for receiving output from the subtraction circuit;

wherein the dc offset estimator and the residual dc offset estimator are fed by output from the A/D converter.

12. A receiver as claimed in any preceding claim comprising a switch for isolating the input and the output of the dc offset estimator after estimation of the dc offset.

13. A method of compensating for dc offset in the baseband signal output of a mixer fed by an incoming signal and a local oscillator signal, comprising:

estimating the dc in the baseband signal in the absence of the incoming signal to the mixer;
storing the estimated dc offset in a register;
estimating residual dc offset in the baseband signal; and
subtracting the stored estimate and the residual dc offset from the baseband signal.

FIG. 1

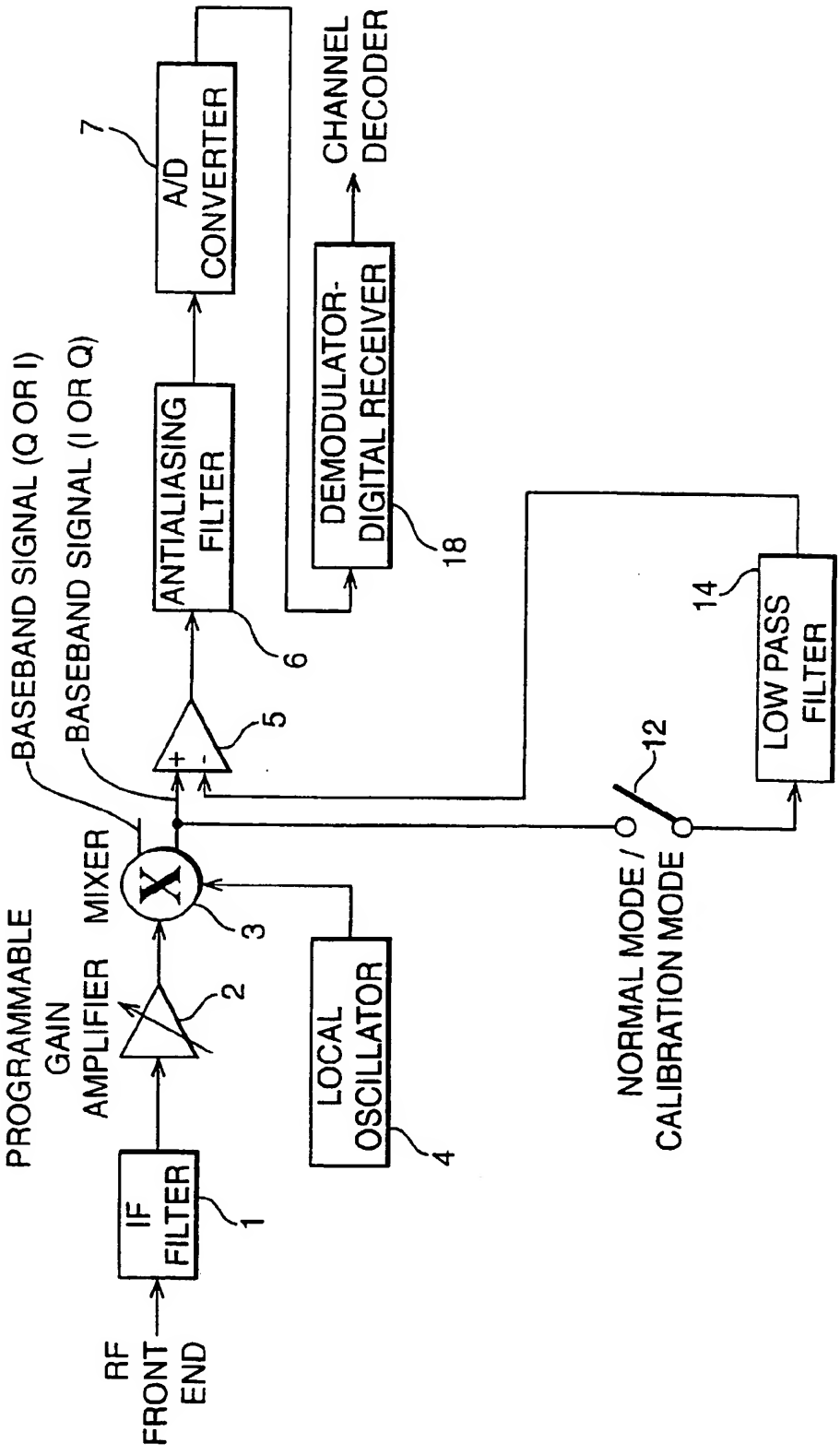

RF FRONT END
IF FILTER
1
PROGRAMMABLE GAIN AMPLIFIER
2
MIXER
3
LOCAL OSCILLATOR
4
BASEBAND SIGNAL (Q OR I)
BASEBAND SIGNAL (I OR Q)
5
+
-
ANTIALIASING FILTER
6
A/D CONVERTER
7
CHANNEL DECODER
DEMODULATOR-DIGITAL RECEIVER
18
NORMAL MODE / CALIBRATION MODE
12
LOW PASS FILTER
14

FIG. 2(A)

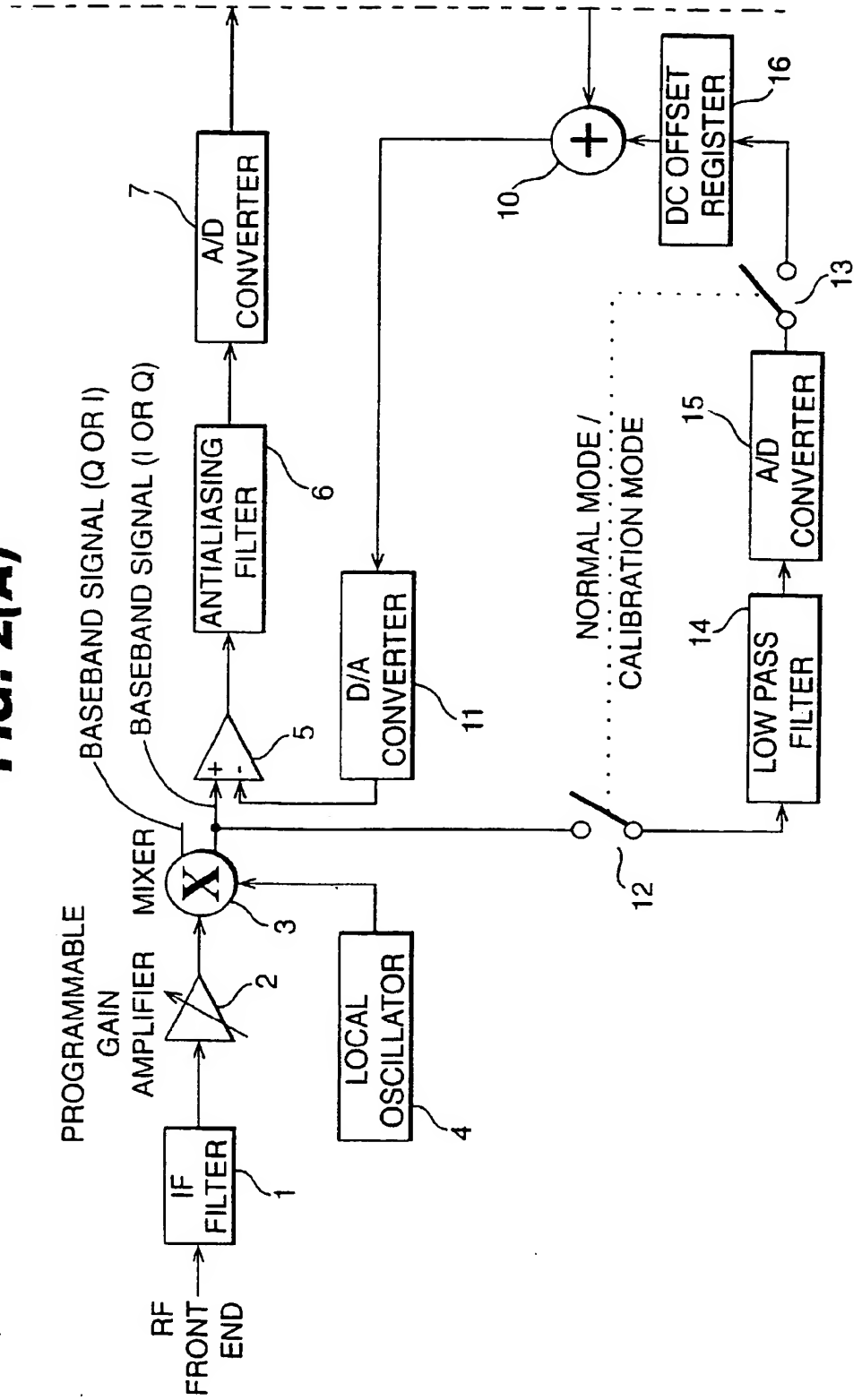

RF FRONT END
IF FILTER
1
PROGRAMMABLE GAIN AMPLIFIER
2
MIXER
3
LOCAL OSCILLATOR
4
BASEBAND SIGNAL (Q OR I)
BASEBAND SIGNAL (I OR Q)
5
ANTIALIASING FILTER
6
A/D CONVERTER
7
D/A CONVERTER
11
10
DC OFFSET REGISTER
16
NORMAL MODE / CALIBRATION MODE
12
13
14
LOW PASS FILTER
15
A/D CONVERTER

FIG.2(B)

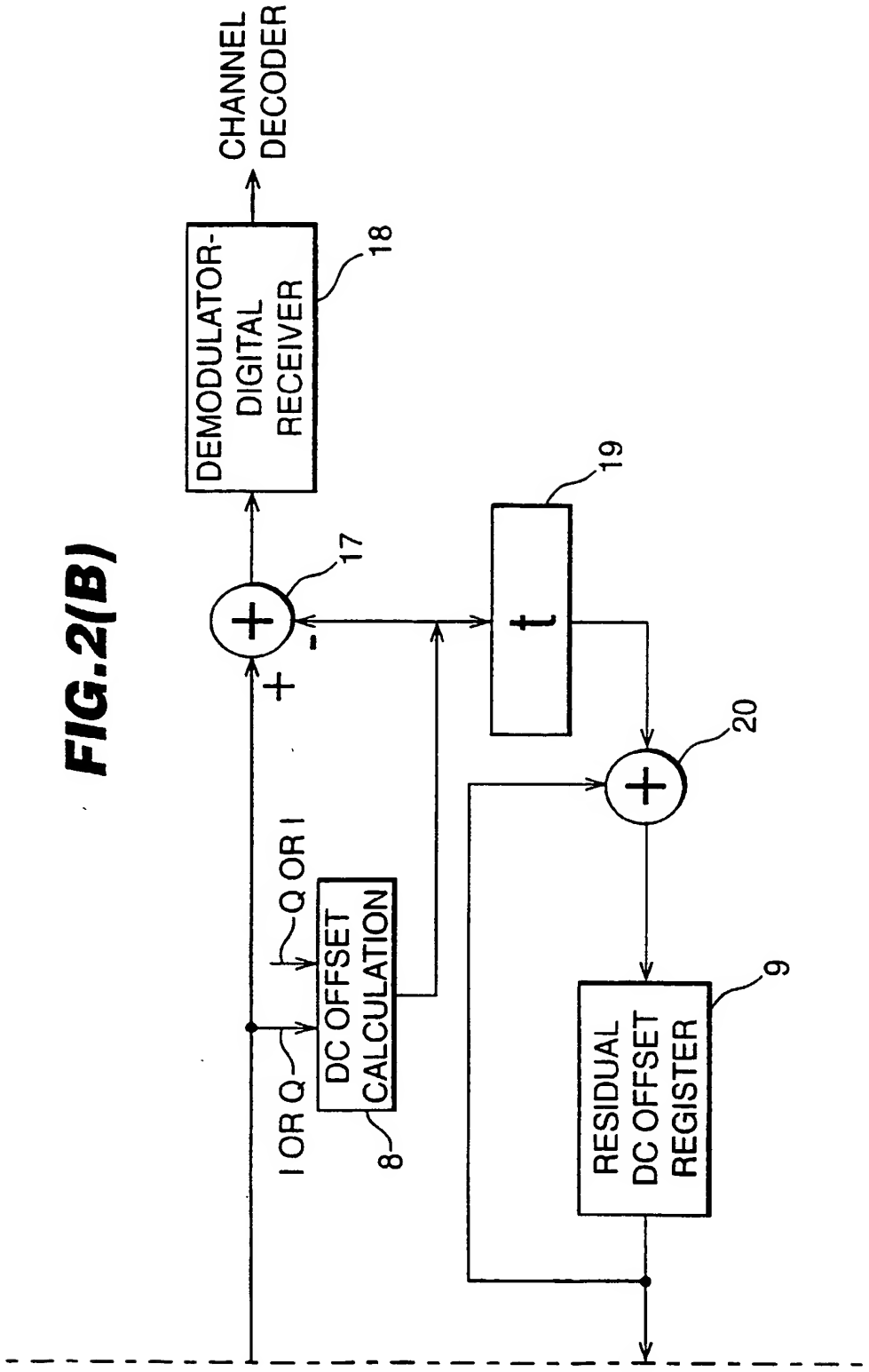

CHANNEL DECODER
DEMODULATOR-DIGITAL RECEIVER
18
19
17
+
-
t
20
+
I OR Q
Q OR I
DC OFFSET CALCULATION
8
RESIDUAL DC OFFSET REGISTER
9

FIG. 2(C)

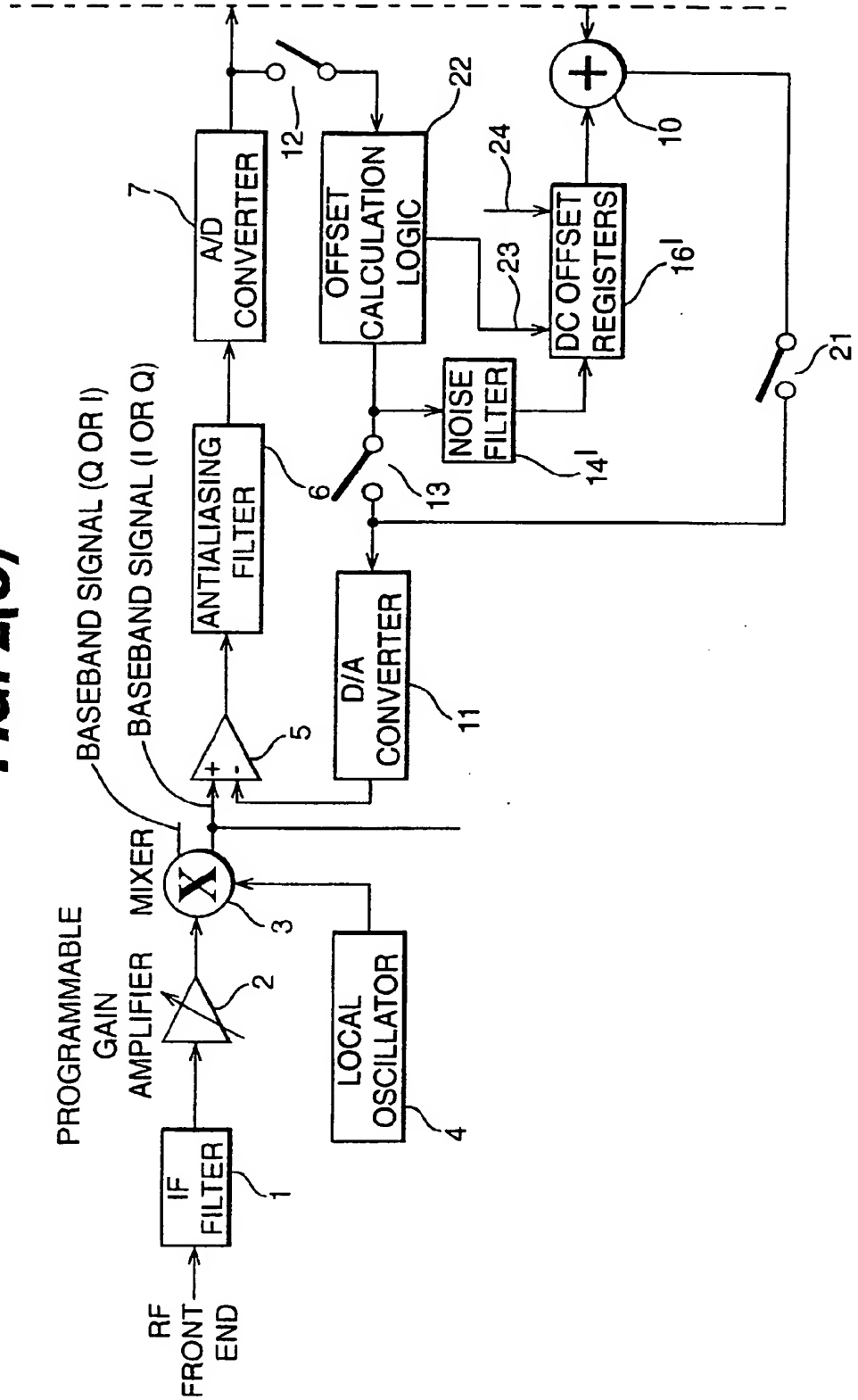
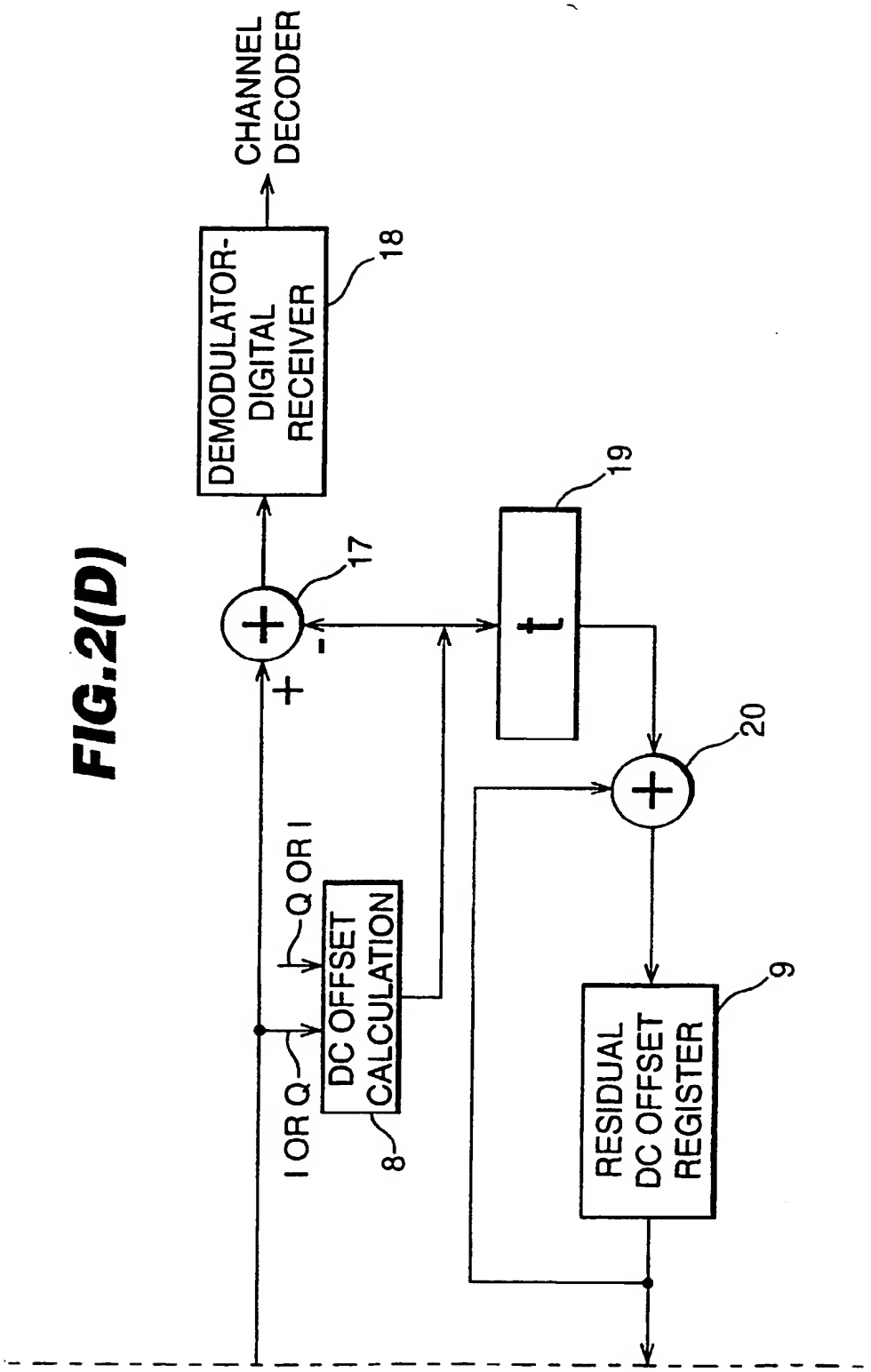

RF FRONT END
IF FILTER
1
PROGRAMMABLE GAIN AMPLIFIER
2
MIXER
3
LOCAL OSCILLATOR
4
BASEBAND SIGNAL (Q OR I)
BASEBAND SIGNAL (I OR Q)
5
ANTIALIASING FILTER
6
A/D CONVERTER
7
D/A CONVERTER
11
12
13
OFFSET CALCULATION LOGIC
22
NOISE FILTER
14
DC OFFSET REGISTERS
16
23
24
10
21

FIG.2(D)


CHANNEL DECODER
DEMODULATOR-DIGITAL RECEIVER
18
19
17
+
-
t
20
Q OR I
I OR Q
DC OFFSET CALCULATION
8
RESIDUAL DC OFFSET REGISTER
9

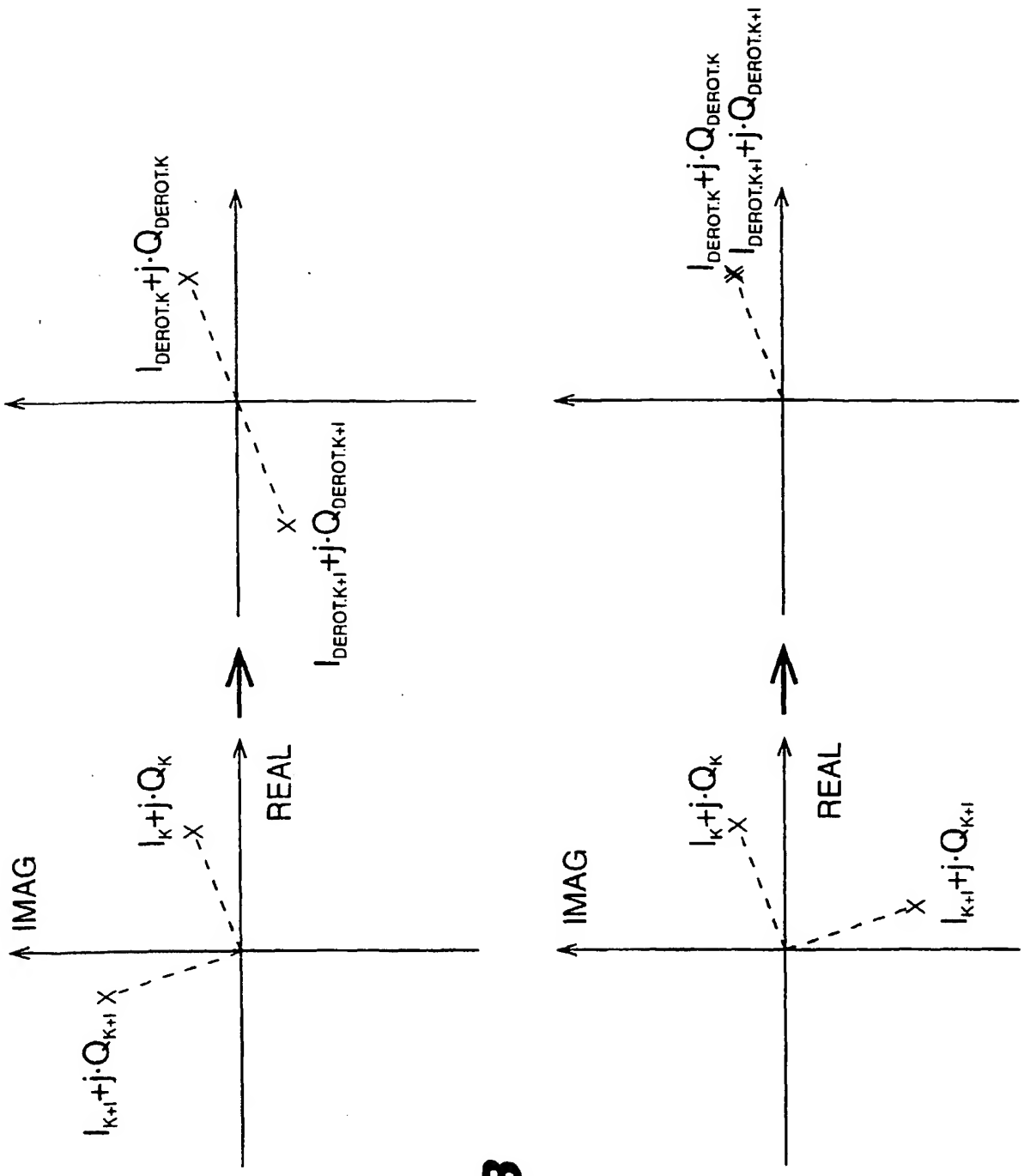

IMAG
REAL
$I_{K+1}+j\cdot Q_{K+1}$
$I_K+j\cdot Q_K$
$I_{DEROT.K}+j\cdot Q_{DEROT.K}$
$I_{DEROT.K+1}+j\cdot Q_{DEROT.K+1}$
IMAG
REAL
$I_{K+1}+j\cdot Q_{K+1}$
$I_K+j\cdot Q_K$
$I_{DEROT.K}+j\cdot Q_{DEROT.K}$
$I_{DEROT.K+1}+j\cdot Q_{DEROT.K+1}$

FIG. 3

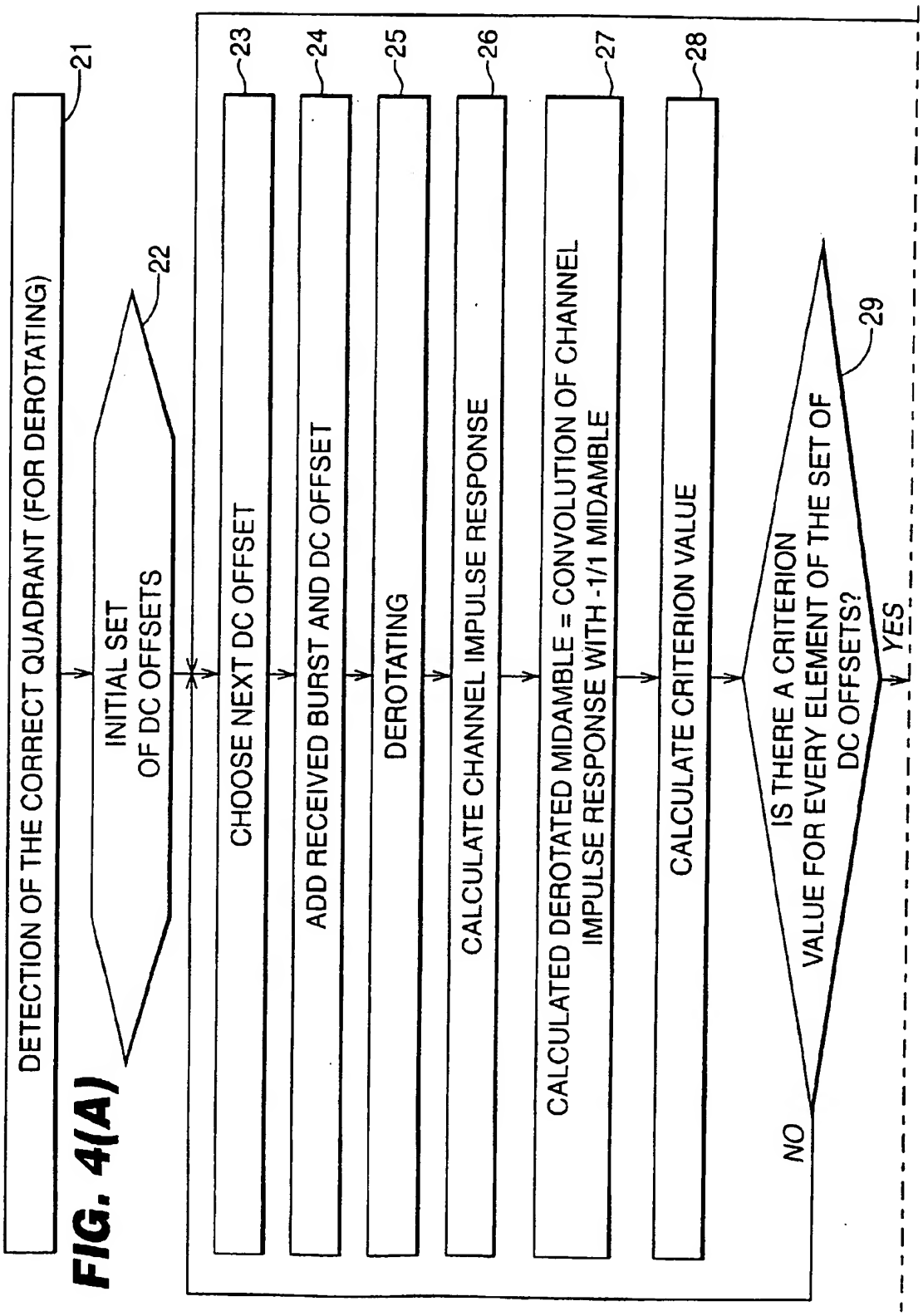

DETECTION OF THE CORRECT QUADRANT (FOR DEROTATING)
21
INITIAL SET OF DC OFFSETS
22
CHOOSE NEXT DC OFFSET
23
ADD RECEIVED BURST AND DC OFFSET
24
DEROTATING
25
CALCULATE CHANNEL IMPULSE RESPONSE
26
CALCULATED DEROTATED MIDAMBLE = CONVOLUTION OF CHANNEL IMPULSE RESPONSE WITH -1/1 MIDAMBLE
27
CALCULATE CRITERION VALUE
28
IS THERE A CRITERION VALUE FOR EVERY ELEMENT OF THE SET OF DC OFFSETS?
29
NO
YES

FIG. 4(A)

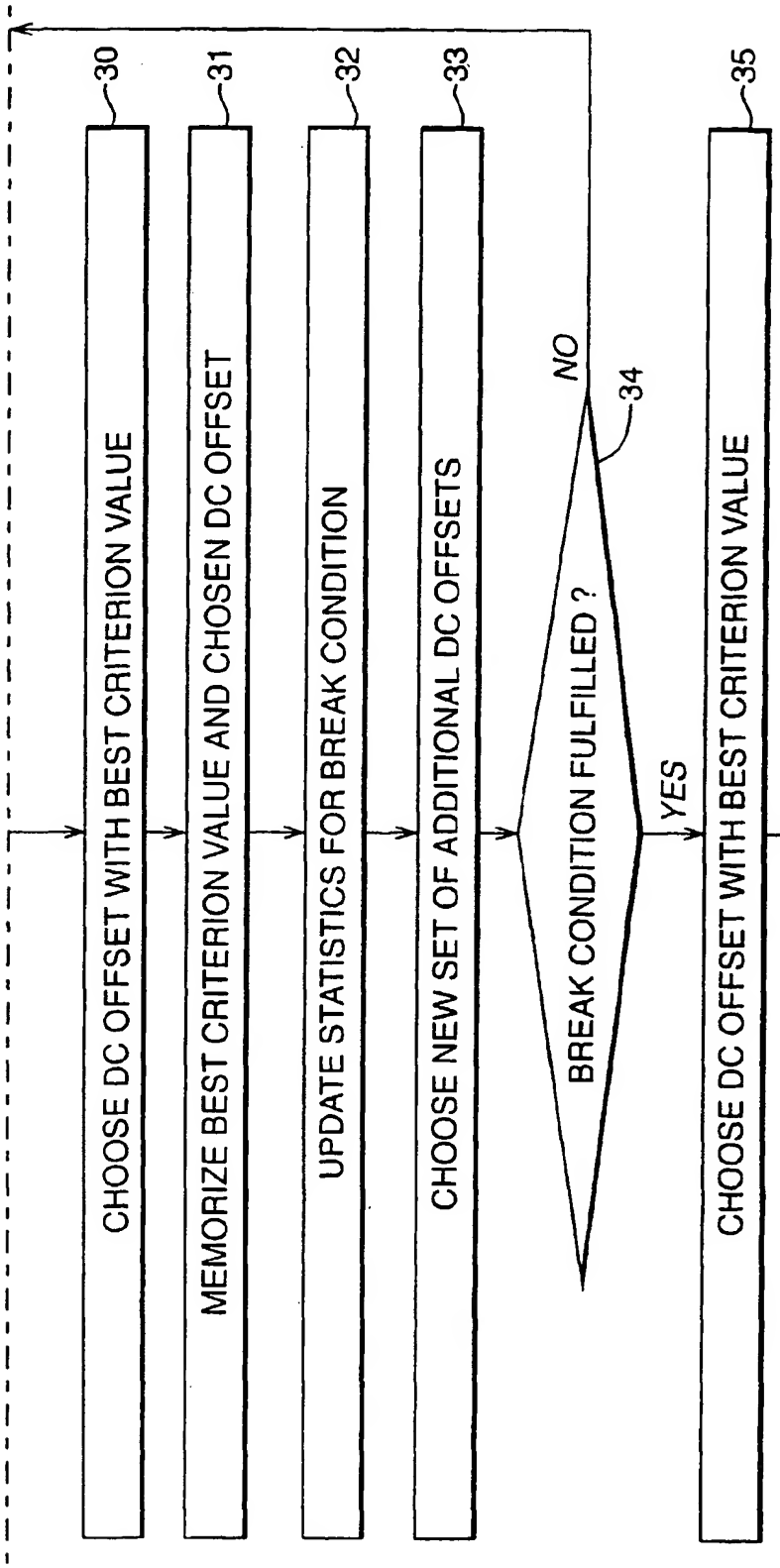

30
CHOOSE DC OFFSET WITH BEST CRITERION VALUE
31
MEMORIZE BEST CRITERION VALUE AND CHOSEN DC OFFSET
32
UPDATE STATISTICS FOR BREAK CONDITION
33
CHOOSE NEW SET OF ADDITIONAL DC OFFSETS
34
BREAK CONDITION FULFILLED ?
NO
YES
35
CHOOSE DC OFFSET WITH BEST CRITERION VALUE
END

FIG. 4(B)

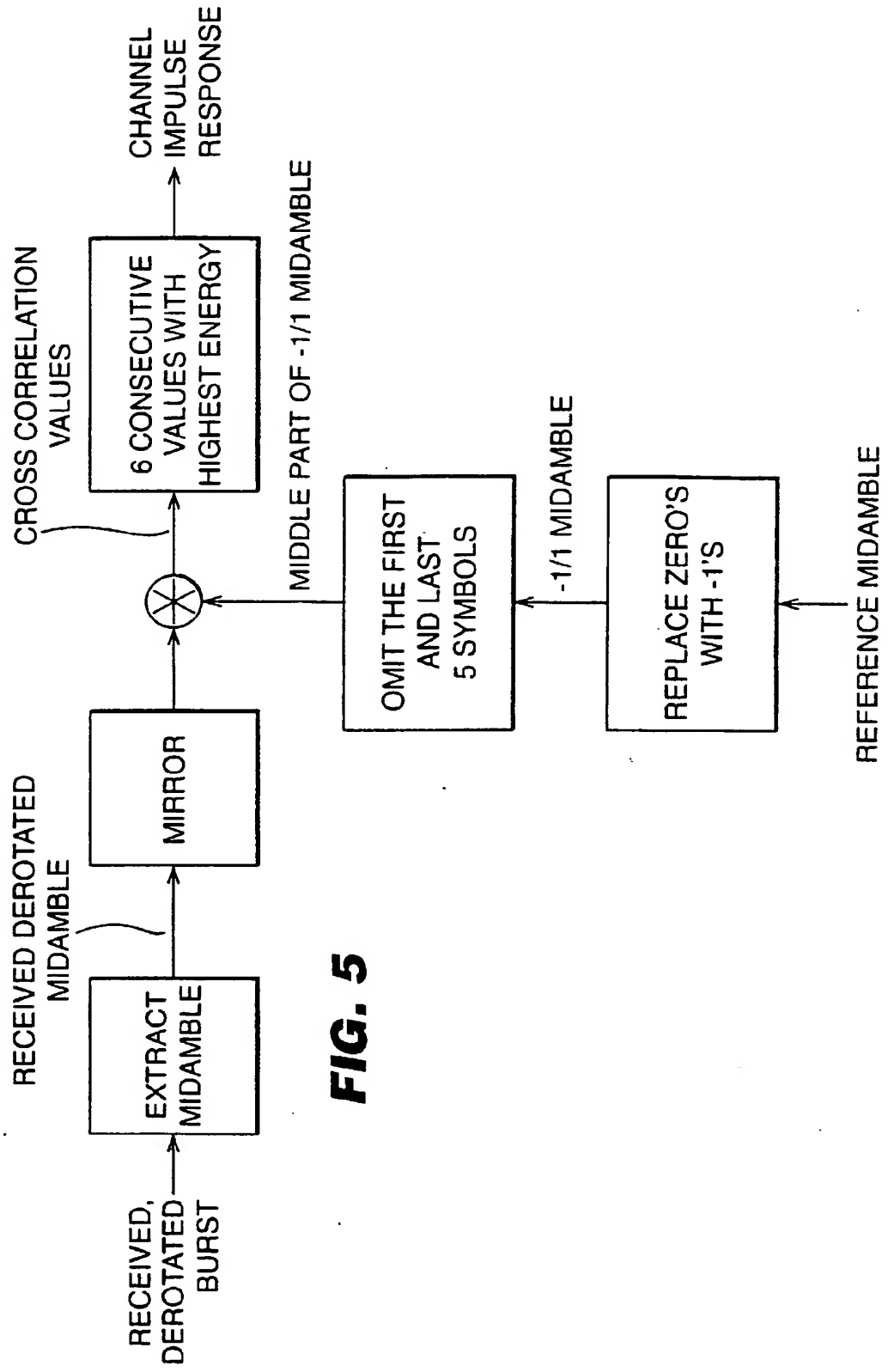

RECEIVED, DEROTATED BURST
EXTRACT MIDAMBLE
RECEIVED DEROTATED MIDAMBLE
MIRROR
CROSS CORRELATION VALUES
6 CONSECUTIVE VALUES WITH HIGHEST ENERGY
CHANNEL IMPULSE RESPONSE
MIDDLE PART OF -1/1 MIDAMBLE
OMIT THE FIRST AND LAST 5 SYMBOLS
-1/1 MIDAMBLE
REPLACE ZERO'S WITH -1'S
REFERENCE MIDAMBLE

FIG. 5

FIG. 6

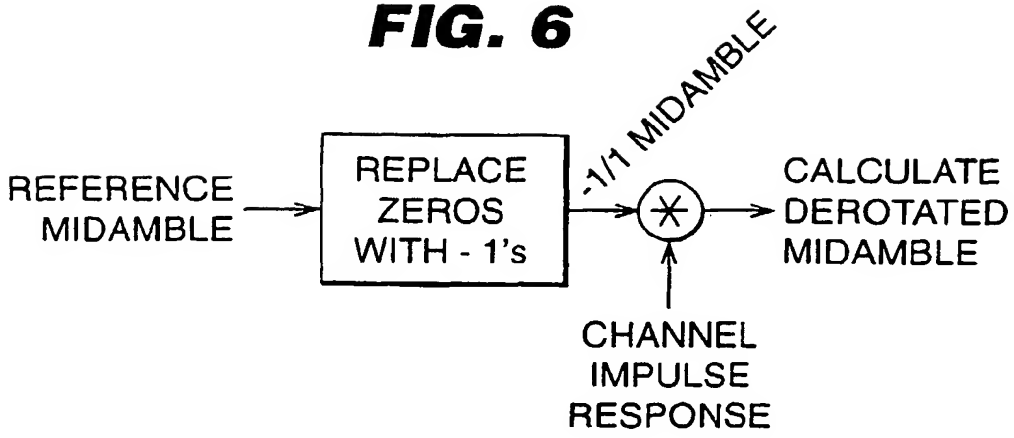


FIG. 7

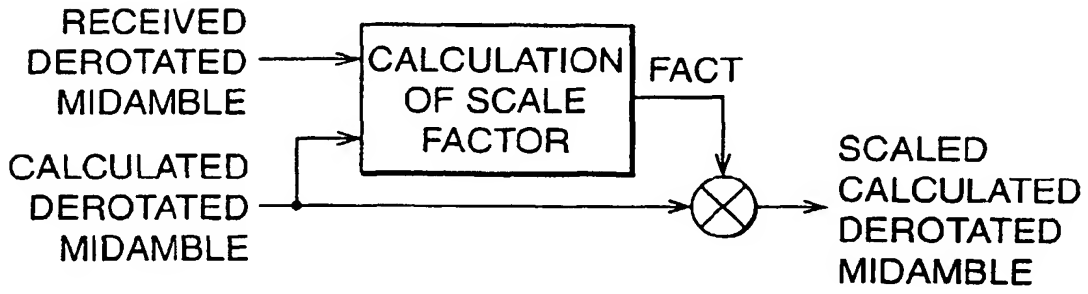
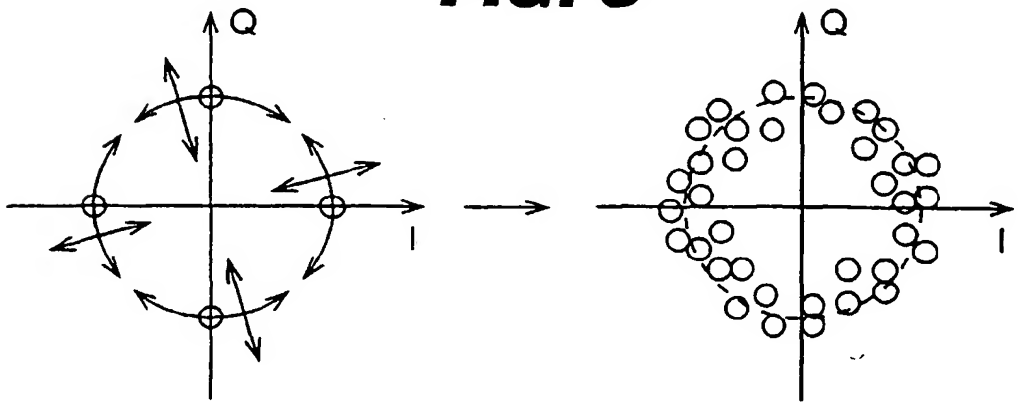


FIG. 8



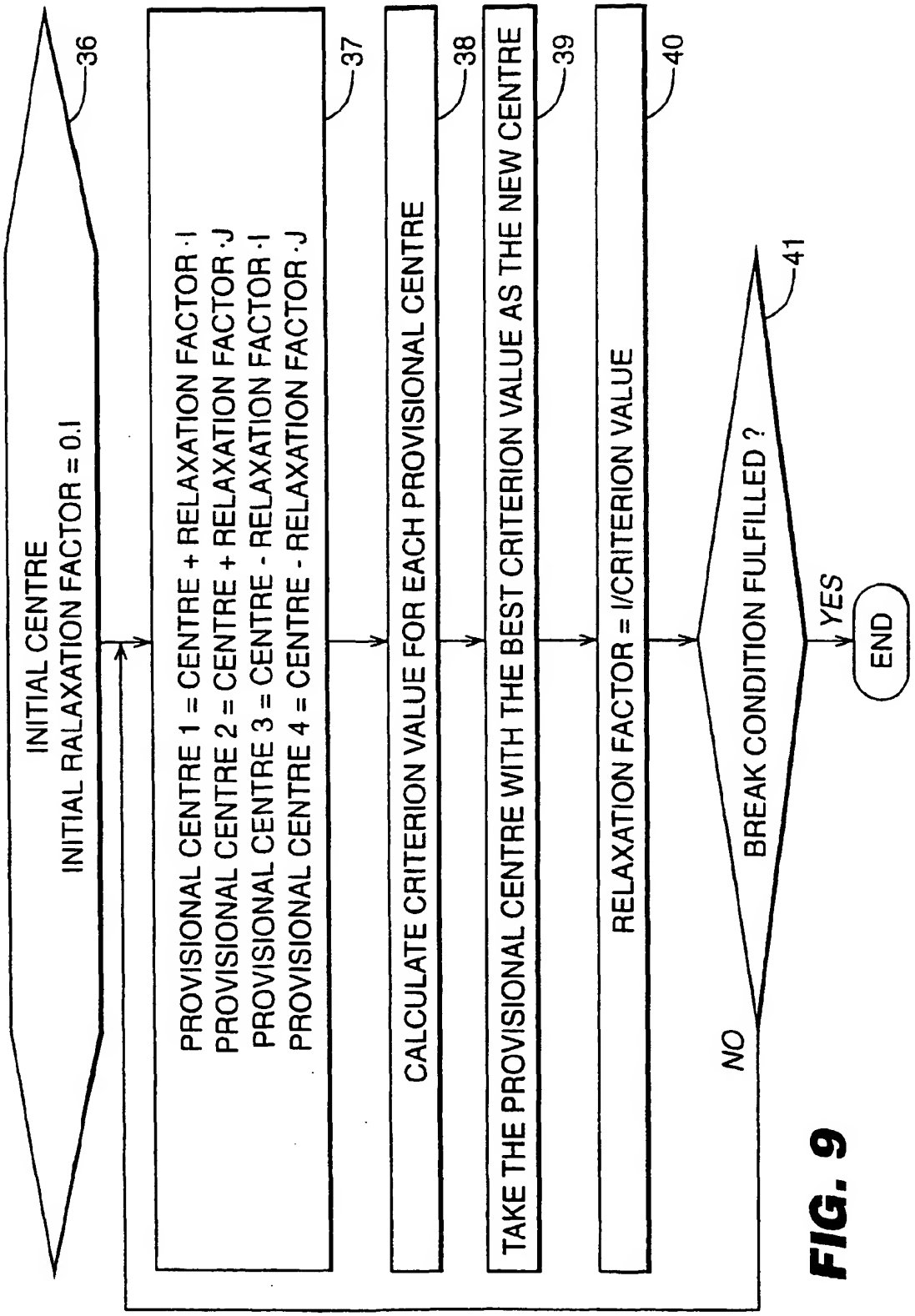

INITIAL CENTRE
INITIAL RALAXATION FACTOR = 0.I
36
PROVISIONAL CENTRE 1 = CENTRE + RELAXATION FACTOR ·I
PROVISIONAL CENTRE 2 = CENTRE + RELAXATION FACTOR ·J
PROVISIONAL CENTRE 3 = CENTRE - RELAXATION FACTOR ·I
PROVISIONAL CENTRE 4 = CENTRE - RELAXATION FACTOR ·J
37
CALCULATE CRITERION VALUE FOR EACH PROVISIONAL CENTRE
38
TAKE THE PROVISIONAL CENTRE WITH THE BEST CRITERION VALUE AS THE NEW CENTRE
39
RELAXATION FACTOR = I/CRITERION VALUE
40
BREAK CONDITION FULFILLED ?
41
NO
YES
END

FIG. 9

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 4097

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
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A	US 5 459 679 A (ZIPEROVICH PABLO A) 17 October 1995 (1995-10-17) * column 8, line 25 - column 10, line 61; figure 2 *	1,4,6-9, 13	
A	WO 95 30275 A (QUALCOMM INC) 9 November 1995 (1995-11-09) * page 17, line 36 - page 18, line 17; figure 9 *	1,13	
A	US 5 748 681 A (HABBAB ISAM M ET AL) 5 May 1998 (1998-05-05) * abstract; figure 1A *	1,13	
A	US 5 663 988 A (NEUSTADT ALF) 2 September 1997 (1997-09-02)		

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H04L
H03D

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	15 September 1999	Peeters, M

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